REMARKS

Claims 18 and 19 are pending in this application. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Claim 18 has been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action.

Rejections under 35 USC §102(b)

Claims 18 and 19 were rejected under 35 USC §102(b) as being anticipated by Yamazaki et al (U.S. Patent No. 5,840,600).

Claim 18, as amended, recites among other things, "wherein the interfacial level density of said semiconductor-insulator junction is 10^{12} $eV^{-1}cm^{-2}$ or less," and "said insulator film is deposited on said underlying semiconductor surface after a treatment that reduces interfacial defects on said semiconductor-insulator junction utilizing a reaction of a treatment gas supplied to the semiconductor substrate having said underlying semiconductor surface via a thermal catalysis body provided near said substrate."

Yamazaki et al discloses a method for producing a semiconductor device. In Yamazaki et al, nothing indicates that "the interfacial level density of said semiconductor-insulator junction is 10^{12} $eV^{-1}cm^{-2}$ or less."

Also, Yamazaki et al describes, for example, as follows:

> The crystalline silicon film 63 undergoes etching to form an island-like silicon film 64 which is the active layer of TFT. **The island-like film 64 and its surrounding area are covered with a silicon oxide film (200-1500 Å thick, typically 1000 Å thick) which is formed by sputtering in an atmosphere of oxygen.** This silicon oxide film functions as the gate insulating film 65. In this example, the sputtering employs a target of synthetic quartz. The sputter gas may be argon. The pressure of the sputter gas is 1 Pa, the electric power applied is 350 W, and the temperature of the substrate is 200°C.
>
> **The gate insulating film 65 undergoes annealing as specified in the present invention. This annealing is intended to improve the characteristics of the interface between the gate insulating film and the active layer.** In this example, the apparatus shown in FIG. 16A is used. The reticulate catalyst 85 is an 80-250 mesh platinum net. The distance between the catalyst 85 and the substrate 84 is 20-80 cm. The gas used for annealing is dinitrogen oxide (100%). The temperature of the heat-annealing furnace 81 is 500°-650°C, typically 550°C. The pressure of the heat-annealing furnace is 0.5-1.1 atm, typically 1 atm. A lower pressure than this is acceptable. The chamber is supplied with dinitrogen oxide at a flow rate of 5 liter/minute. The heat annealing lasts for 0.5-6 hours, typically 1 hour. As the result of this treatment, the amount of hydrogen at the interface between the silicon oxide film and the silicon film is reduced by nitriding or oxidation and conversely the amount of nitrogen at the interface is increased. (FIG. 17B)

(Column 31, lines 24-52, emphasis added). In Yamazaki et al, annealing is conducted after the insulating film is formed. That means that the insulator film is deposited on said underlying semiconductor surface **before the heat treatment**.

Thus, Yamazaki et al does not teach or suggest "wherein the interfacial level density of said semiconductor-insulator junction is 10^{12} $eV^{-1}cm^{-2}$ or less," and "said insulator film is deposited on said underlying semiconductor surface after a treatment that reduces interfacial defects on said semiconductor-insulator junction utilizing a reaction of a treatment gas supplied to the semiconductor substrate having said underlying semiconductor surface via a thermal catalysis body provided near said substrate," as recited in amended claim 18.

Reference Drawing 1 shows that etching rate of silicon by hydrogen made by catalytic reaction. As shown in Reference Drawing 1, silicon is easily etched while silicon oxide and silicon nitride are not etched.

During a film deposition, material adsorbing on the surface forms many small islands in the initial stage. Then, with the accumulation of the material, the islands grow to form a film. In the process of Yamazaki et al, because insulator film deposition is carried out onto a semiconductor surface which is not oxidized or nitrided, many small islands are formed on the semiconductor surface causing differences in etching resistivity between areas covered with the islands and areas not covered with them.

These result in a rugged surface on the semiconductor, where etching is concentrated on areas where the islands are not formed. The film is deposited on such rugged surface. Such a structural unevenness increases the interfacial level density. The process of Yamazaki et al inevitably accompanies this problem. Therefore, Yamazaki et al does not satisfy, among other things, "wherein the interfacial level density of said semiconductor-insulator junction is 10^{12} $eV^{-1}cm^{-2}$ or less."

In contrast, the present invention is free from such a problem. The difference of the results is not expected, because Yamazaki et al does not teach or suggest the broad technical concept "interfacial level density." Also, Yamazaki et al does not discuss the relationship between the unevenness and interfacial level density.

Moreover, the improvement in device property by Yamazaki et al is limited. Because the treatment of Yamazaki et al is conducted after the insulator film deposition, reactive material has to travel through the deposited insulator film to reach the interface onto the underlying semiconductor and improve the property of the interface.

Reference Drawing 2 compares capacity-voltage (C-V) characteristics between the silicon nitride film directly deposited on the silicon (shown by square dots) and silicon nitride film deposited after exposing the silicon surface to radicals obtained by catalytically decomposing ammonia gas (shown by round dots). The former has significant hysteresis in C-V characteristics, and the threshold voltage of the former deviates far from 0V. These facts shows the existence of charge-injected defects and fixed charges. In contrast,

the latter shows very little hysteresis and little deviation of the threshold voltage from 0V. Thus, Reference Drawing 2 shows that nitridation of silicon surface before deposition of silicon nitride is effective to reduce threshold voltage shift and also width of hystelysis loop.

Reference Drawing 3 shows high resolution transmission electron microscopy (HRTEM) images of an interface with nitridation and one without nitridation. Reference Drawing 3 clearly shows that (silicon)/(silicon nitride) surface becomes leveled by the treatment before deposition, in other words, that unevenness results if such treatment is not performed.

Yamazaki et al teaches or suggests none of these discoveries of the present inventors. For at least these reasons, claim 18 patentably distinguishes over Yamazaki et al.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosure: Reference Drawings 1-3

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